United States Patent [19]

McClure

[11] **Patent Number: 5,019,724**

[45] **Date of Patent: May 28, 1991**

[54] **NOISE TOLERANT INPUT BUFFER**

[75] Inventor: **David C. McClure**, Carrollton, Tex.

[73] Assignee: **SGS-Thomson Microelectronics, Inc.**, Carrollton, Tex.

[21] Appl. No.: **453,589**

[22] Filed: **Dec. 20, 1989**

[51] **Int. Cl.**[5] **H03K 5/22**; H03K 17/16

[52] **U.S. Cl.** **307/443**; 307/592; 307/594

[58] **Field of Search** 307/443, 592, 594, 542.1, 307/272.2, 601, 480, 481, 265

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,710,648	12/1987	Hanamura et al.	307/443
4,717,835	1/1988	Takeuchi	307/480
4,760,279	5/1988	Saito et al.	307/443

FOREIGN PATENT DOCUMENTS

0032824	4/1981	Japan	307/443

Primary Examiner—David Hudspeth
Assistant Examiner—Andrew Sanders
Attorney, Agent, or Firm—Dennis T. Griggs; Richard K. Robinson

[57] **ABSTRACT**

An input buffer interface circuit provides high state and low state input noise tolerance by a tri-state CMOS inverter having high state and low state inputs which are driven conditionally after the propagation of an input signal through predetermined high state and low state delay circuits. In one embodiment, a resettable high state delay circuits is provided by a cascaded combination of NOR gates and inverters, whereby the delay is preempted automatically by an excursion from high to low with the result that the delay path is reinitialized automatically for rejection of successive high state ringing fluctuations. A resettable low state delay circuit is provided by a cascaded combination of NAND gates and inverters.

16 Claims, 2 Drawing Sheets