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# United States Patent [19]

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Queyssac et al.

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[54] **METHOD FOR PACKAGING AN ELECTRONIC CIRCUIT DEVICE**

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[57] **ABSTRACT**

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An integrated circuit package encapsulates a volatile memory chip and a backup battery for preserving data in the event of loss of main power supply. The package includes a finger lead assembly encapsulated within a body of non-conductive material, with a central base support finger lead being offset within an interconnect region. One terminal of the battery is welded to the offset base finger lead, and the integrated circuit chip is bonded directly onto the other battery terminal by a layer of conductive epoxy. The stacked assembly of the integrated circuit chip, the battery and the offset base finger lead is centered longitudinally and vertically within the interconnect region whereby the stacked assembly, including gold interconnect wires, are completely encapsulated within the molded package body, without increasing the standoff height of the package.

**Related U.S. Application Data**

[62] Division of Ser. No. 534,151, Jun. 6, 1990, Pat. No. 5,089,877.

[51] Int. Cl.<sup>5</sup> ..... **H01R 43/00**

[52] U.S. Cl. .... **29/827**; 179/52.4;  
257/678; 368/88

[58] Field of Search ..... 368/88; 357/75; 29/852,  
29/827; 174/52.4

[56] **References Cited**

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**1 Claim, 5 Drawing Sheets**

